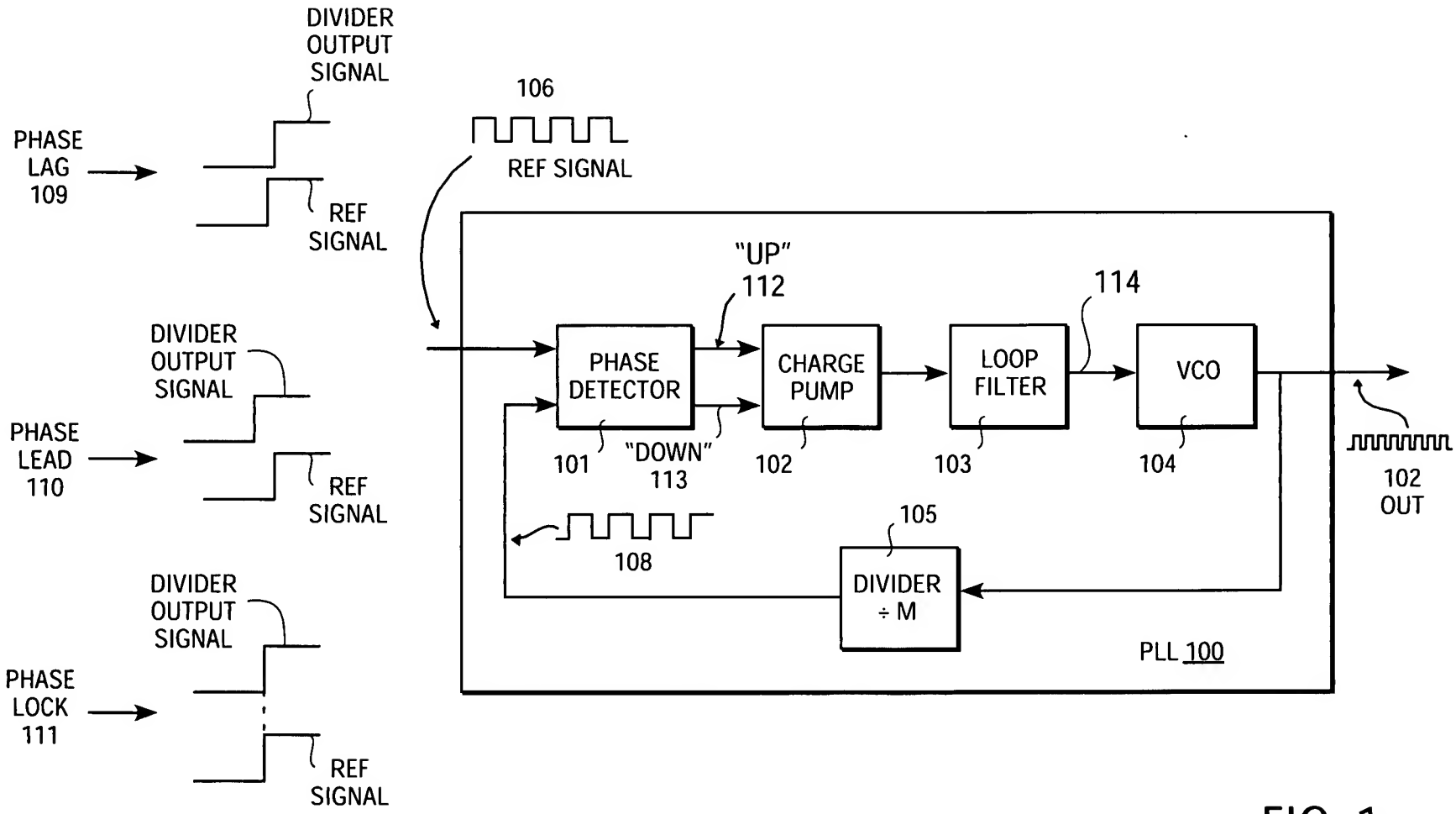

DIVIDER OUTPUT SIGNAL
PHASE LAG 109
REF SIGNAL
106
REF SIGNAL
"UP" 112
114
DIVIDER OUTPUT SIGNAL
PHASE LEAD 110
REF SIGNAL
PHASE DETECTOR
CHARGE PUMP
LOOP FILTER
VCO
101
"DOWN" 113
102
103
104
102 OUT
108
105
DIVIDER OUTPUT SIGNAL
PHASE LOCK 111
DIVIDER ÷ M
REF SIGNAL
PLL 100

FIG. 1

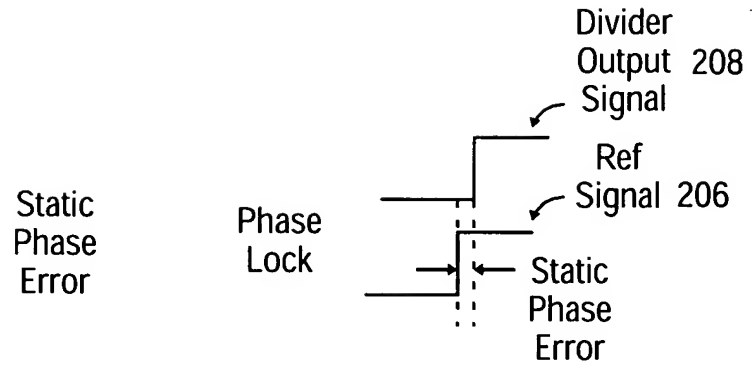



FIG. 2A

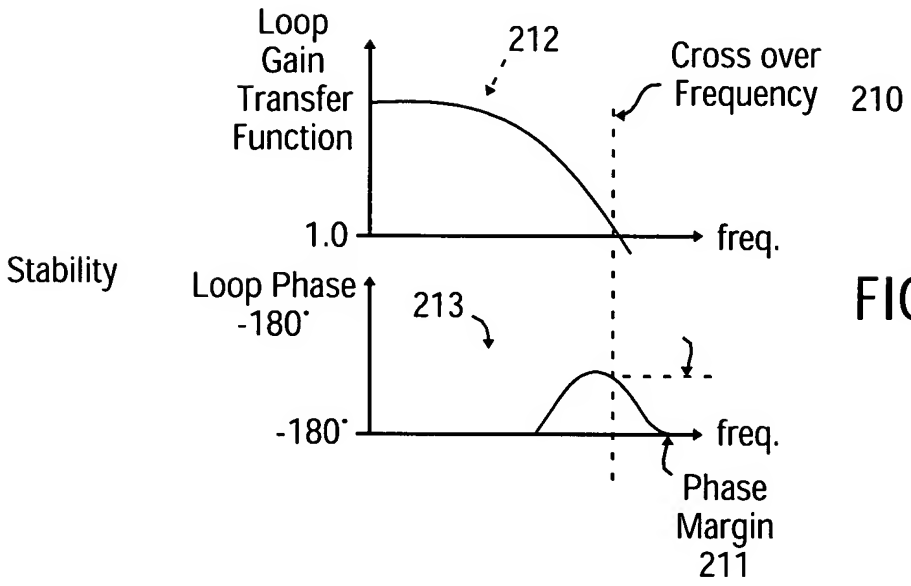



FIG. 2B

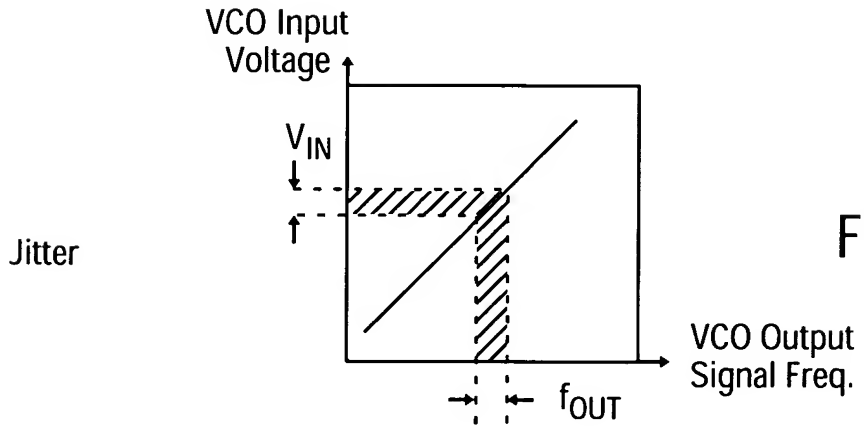



FIG. 2C

301

M1 = PMOS; GATE WIDTH = $W_1$; GATE LENGTH = $L_1$
M2 = PMOS; GATE WIDTH = $W_2$; GATE LENGTH = $L_2$
M3 = NMOS; GATE WIDTH = $W_3$; GATE LENGTH = $L_3$
M4 = NMOS; GATE WIDTH = $W_4$; GATE LENGTH = $L_4$
M5 = PMOS; GATE WIDTH = $W_5$; GATE LENGTH = $L_5$
M6 = NMOS; GATE WIDTH = $W_6$; GATE LENGTH = $L_6$
M7 = PMOS; GATE WIDTH = $W_7$; GATE LENGTH = $L_7$
M8 = PMOS; GATE WIDTH = $W_8$; GATE LENGTH = $L_8$

$I_{BIAS}$ = I AMPS
$R_C$ = R OHMS
$C_C$ = C CARADS

302

1 = $V_{DD}$; $M8_{SOURCE}$; $M5_{SOURCE}$; $M7_{SOURCE}$
2 = $M1_{GATE}$
3 = $M2_{GATE}$
4 = $C_C2$; $M6_{DRAIN}$; $M7_{DRAIN}$
5 = $M5_{GATE}$; $M7_{GATE}$; $M8_{GATE}$; $I_{BUS\ 1}$
6 = $M1_{SOURCE}$; $M2_{SOURCE}$; $M5_{DRAIN}$
7 = $M1_{DRAIN}$; $M3_{DRAIN}$; $M3_{GATE}$; $M4_{GATE}$
8 = $M2_{DRAIN}$; $R_{C1}$; $M4_{DRAW}$; $M6_{GATE}$
9 = $R_C$ 2; $C_C$ 2
10 = $V_{SS}$; $I_{BUS\ 2}$; $M3_{SOURCE}$; $M4_{SOURCE}$; $M6_{SOURCE}$

300

FIG. 3A

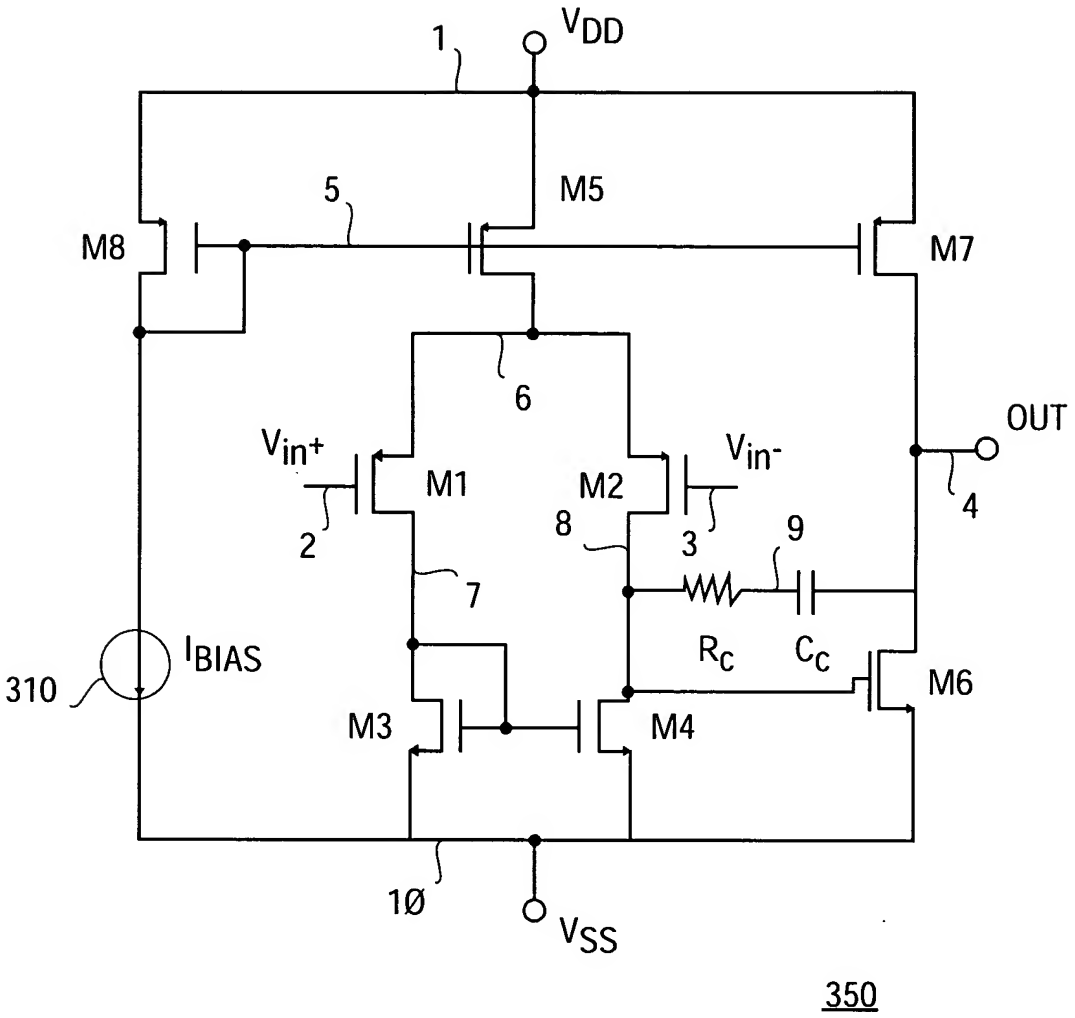

1
VDD
5
M5
M8
M7
6
OUT
Vin+
M1
M2
Vin-
2
8
3
9
4
7
IBIAS
310
Rc
Cc
M6
M3
M4
1Ø
VSS
350

FIG. 3B

- SILICON SURFACE AREA CONSUMPTION = A $CM^2$
- POWER CONSUMPTION = B mW
- OPEN LOOP GAIN = C dB
- UNITY GAIN BANDWIDTH = D $MH_Z$
- SLEW RATE = E $V/_{nsec}$

•
•
•
•

400

FIG. 4A

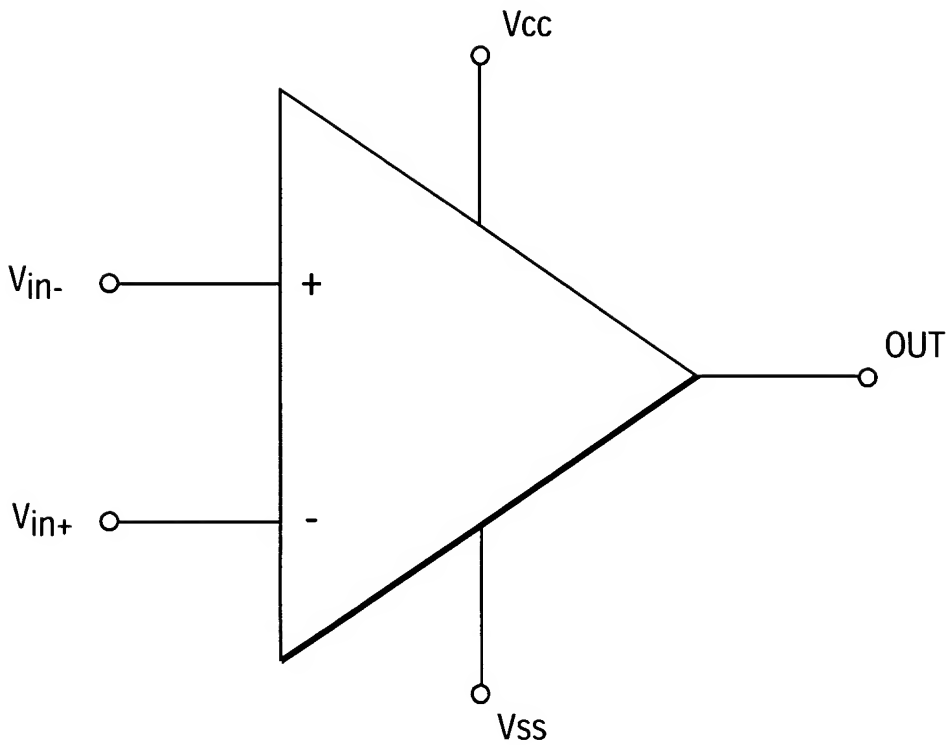



FIG. 4B

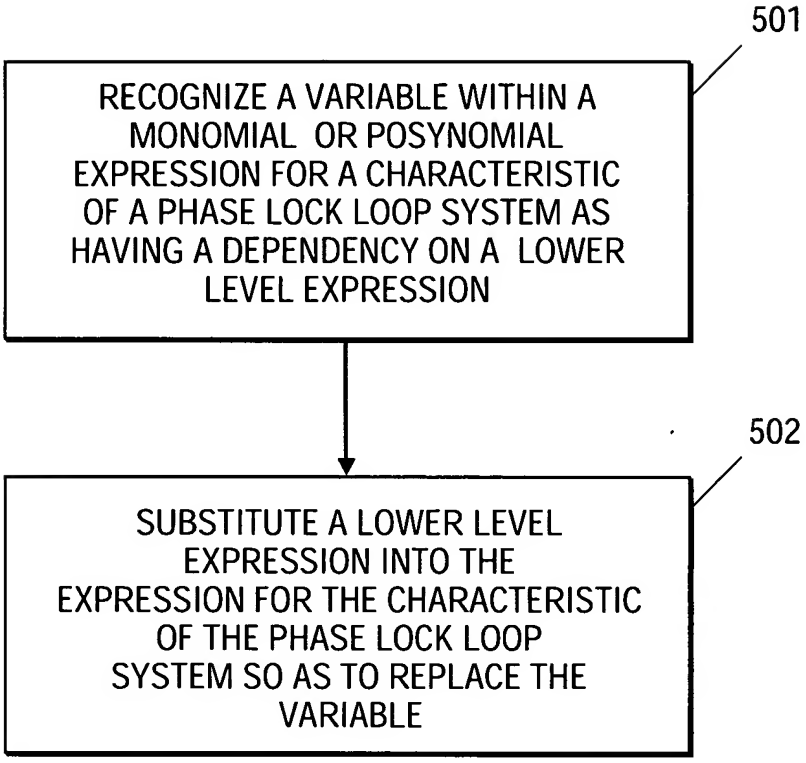

501
RECOGNIZE A VARIABLE WITHIN A MONOMIAL OR POSYNOMIAL EXPRESSION FOR A CHARACTERISTIC OF A PHASE LOCK LOOP SYSTEM AS HAVING A DEPENDENCY ON A LOWER LEVEL EXPRESSION
502
SUBSTITUTE A LOWER LEVEL EXPRESSION INTO THE EXPRESSION FOR THE CHARACTERISTIC OF THE PHASE LOCK LOOP SYSTEM SO AS TO REPLACE THE VARIABLE
500

FIG. 5A

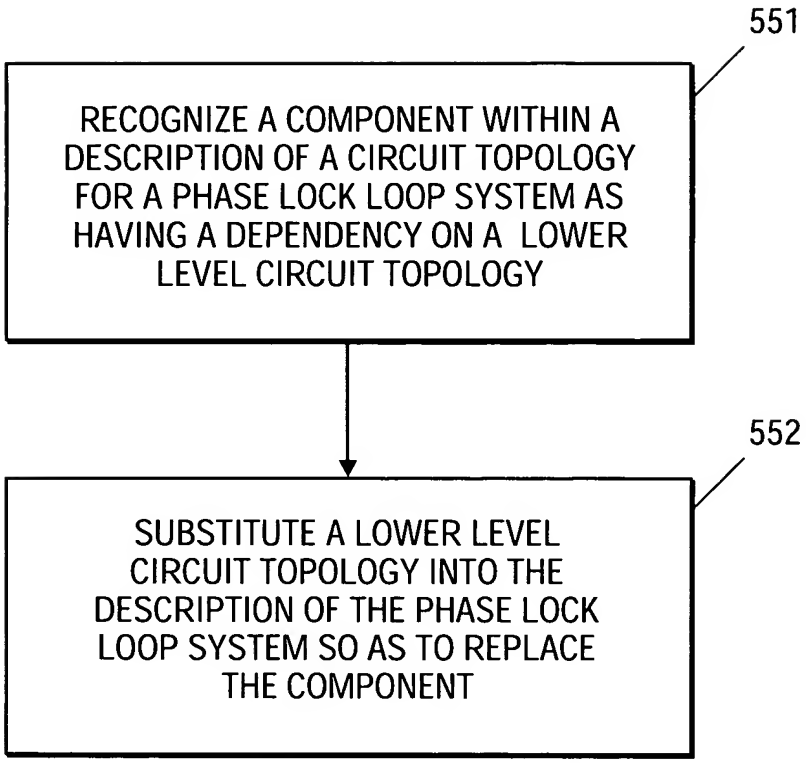
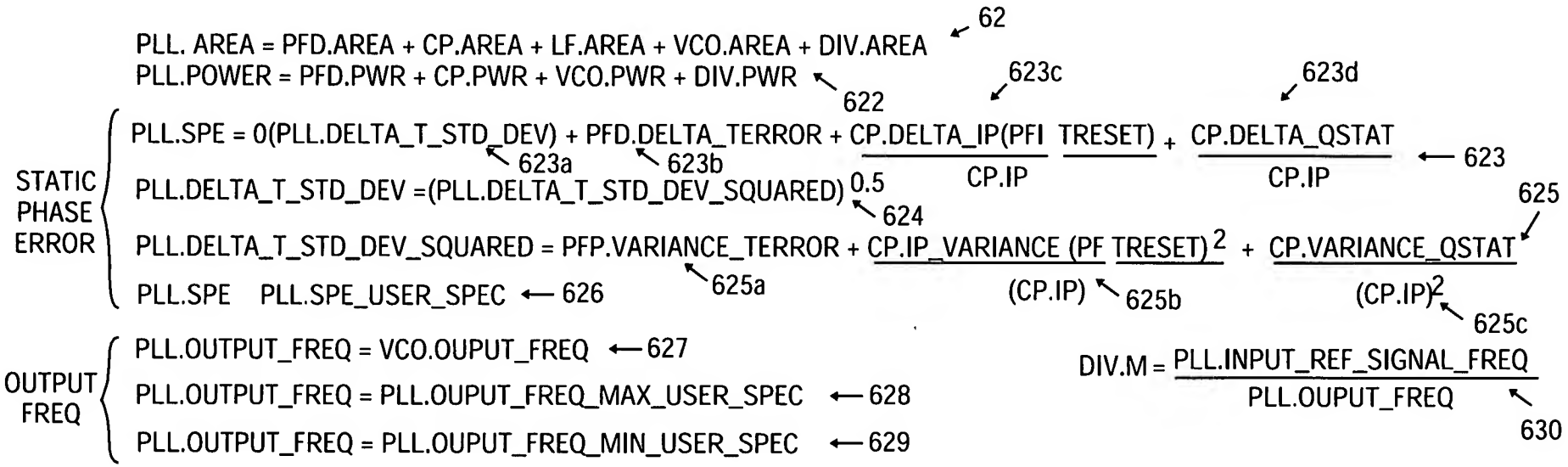

551
RECOGNIZE A COMPONENT WITHIN A DESCRIPTION OF A CIRCUIT TOPOLOGY FOR A PHASE LOCK LOOP SYSTEM AS HAVING A DEPENDENCY ON A LOWER LEVEL CIRCUIT TOPOLOGY
552
SUBSTITUTE A LOWER LEVEL CIRCUIT TOPOLOGY INTO THE DESCRIPTION OF THE PHASE LOCK LOOP SYSTEM SO AS TO REPLACE THE COMPONENT
550

FIG. 5B




PLL SYSTEM
LEVEL EQUATIONS
600A

FIG. 6A

# FIG. 6A (CONT.)

PLL SYSTEM LEVEL EQUATIONS 600A

STABILITY

$$PLL.CROSS\_OVER\_FREQ = \frac{LF.R(PFD.GAIN)\,(CP.IP)\,(VCD.GAIN)}{DIV.M} \leftarrow 631$$

$$PLL.PHASE\_MARGIN = /2 - \frac{1}{PLL.CROSS\_OVER\_FREQ\,(LF.R)\,(LF.C2)} - PLL.CROSS\_OVER\_FREQ\,(LF.R)\,(LF.C2) \} 632$$

$$-PLL.CROSS\_OVER\_FREQ\,(VCD.TAV3)$$

$$PLL.CROSS\_OVER\_FREQ \quad PLL.CROSS\_OVER\_FREQ\_USER\_SPEC \leftarrow 633$$

$$PLL.PHASE\_MARGIN \quad PLL.PHASE\_MARGIN\_USER\_SPEC \leftarrow 634$$

635

PEAK JITTER

$$PLL.PEAK\_JITTER = \frac{VCO.KAPPA\,(2\ )^{0.5}\,(DIV.M)^{0.5}\,(LF.C1)^{0.5}}{(PFD.GAIN)^{0.5}\,(CP.IP)^{0.5}\,(VCO.GAIN)^{0.5}} \leftarrow 635a +$$

$$+ \frac{3(SIA[\ (SEC.TRESET)\,(PLL.INPUT\_REF\_SIGNAL\_FREQ)])\,(CP.DELTA\_IP)\,ICO.GAIN)\,(LF.R)}{2\,(PLL.INPUT\_REF\_SIGNAL\_FREQ)\,(DIV.1)} \quad \overbrace{\propto (LF.R)\,(LF.C2)\,2\ \ (PLL.INPUT\_REF\_SIGNAL\_FREQ)?}^{635b1}$$

635b

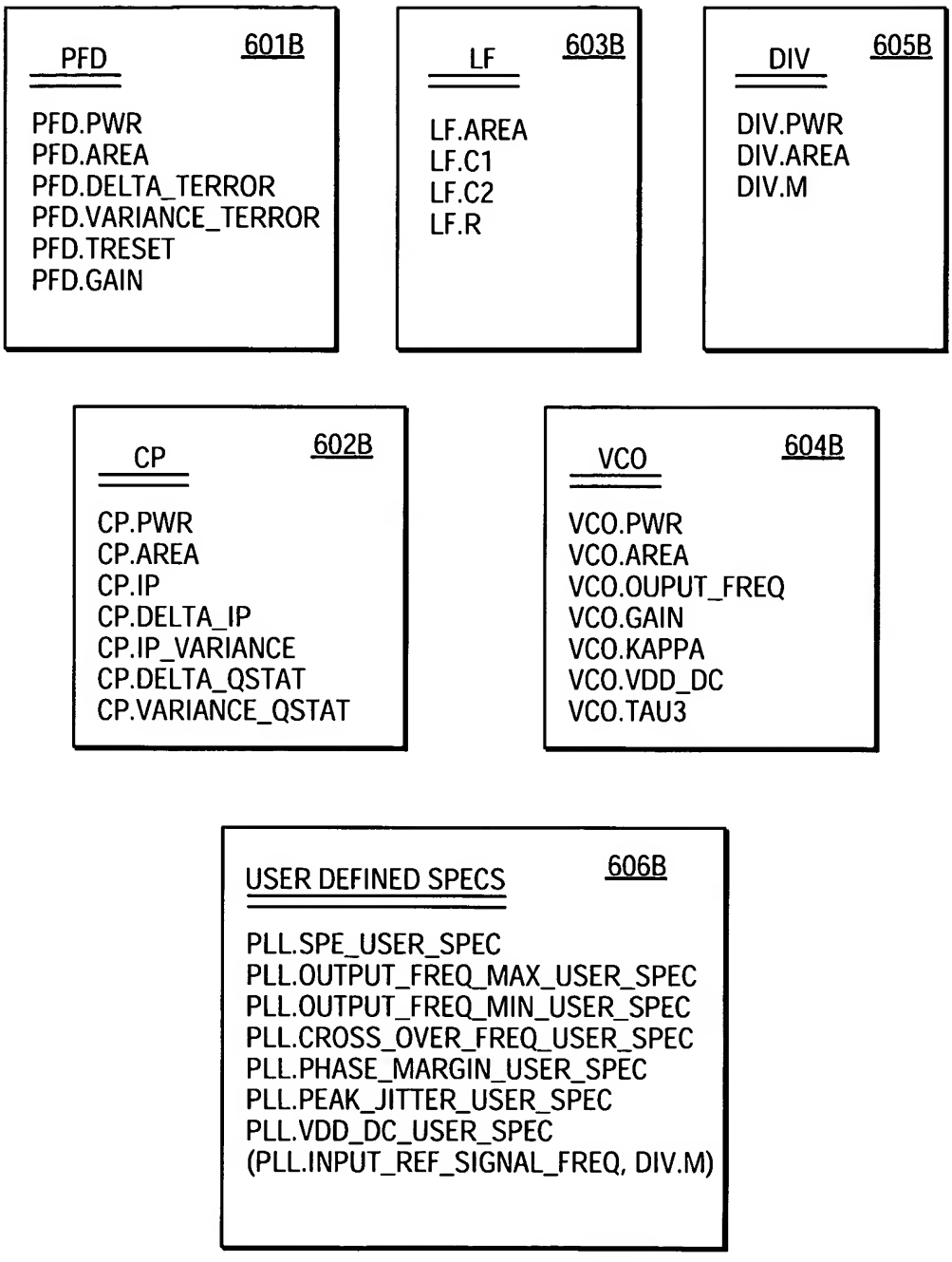
$$PLL.PEAK\_JITTER \quad PLL.PEAK\_JITTER\_USER\_SPEC \leftarrow 636$$

POWER SUPPLY REJECTION

$$PLL.VDD\_DC = VCO.VDD\_DC \leftarrow 637$$

$$PLL.VDD\_DC \quad PLL.VDD\_DC\_USER\_SPEC \leftarrow 638$$

600B




PLL SYSTEM
LEVEL VARIABLES

FIG. 6B

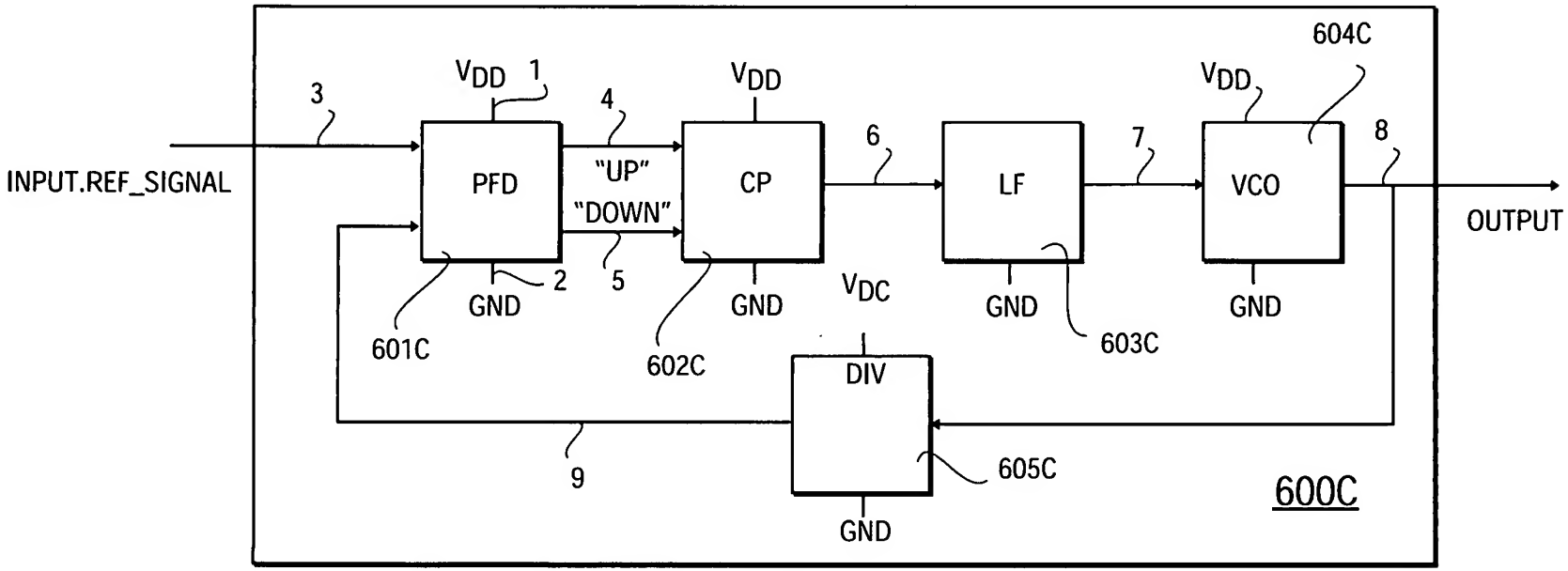

INPUT.REF_SIGNAL
3
PFD
$V_{DD}$ 1
GND 2
601C
4
"UP"
"DOWN"
5
CP
$V_{DD}$
GND
602C
6
LF
GND
603C
7
VCO
$V_{DD}$
604C
GND
8
OUTPUT
$V_{DC}$
DIV
605C
GND
9
600C

FIG. 6C

PFD

CP

LF

VCO

DIV

1 = PFD.VDD; CP.VDD; VCO.VDD; DIV.VDD

2 = PFD.GND; CP.GND; LF.GND; VCO.GND; DIV.GND

3 = PFD.IN_1

4 = PFD.OUT_UP; CP.IN_UP

5 = PFD.OUT_DOWN; CP.IN_DOWN

6 = CP.OUT; LF.IN

7 = LF.OUT; VCO.IN

8 = VCO.OUT; DIV.IN

9 = DIV.OUT; PFD.IN_2

FIG. 6D

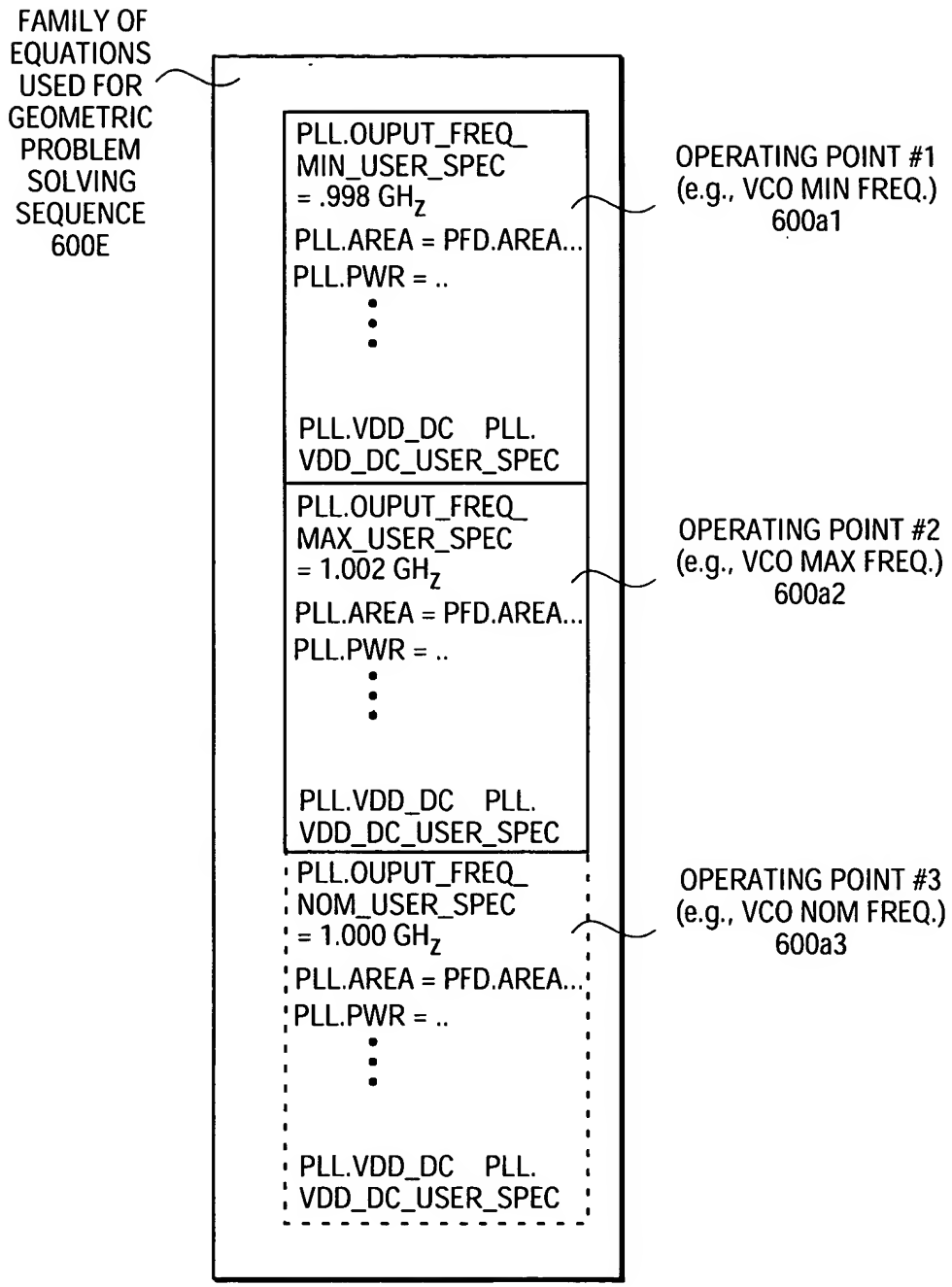

FAMILY OF EQUATIONS USED FOR GEOMETRIC PROBLEM SOLVING SEQUENCE 600E
PLL.OUPUT_FREQ_ MIN_USER_SPEC = .998 GHz
PLL.AREA = PFD.AREA...
PLL.PWR = ..
PLL.VDD_DC PLL. VDD_DC_USER_SPEC
OPERATING POINT #1 (e.g., VCO MIN FREQ.) 600a1
PLL.OUPUT_FREQ_ MAX_USER_SPEC = 1.002 GHz
PLL.AREA = PFD.AREA...
PLL.PWR = ..
PLL.VDD_DC PLL. VDD_DC_USER_SPEC
OPERATING POINT #2 (e.g., VCO MAX FREQ.) 600a2
PLL.OUPUT_FREQ_ NOM_USER_SPEC = 1.000 GHz
PLL.AREA = PFD.AREA...
PLL.PWR = ..
PLL.VDD_DC PLL. VDD_DC_USER_SPEC
OPERATING POINT #3 (e.g., VCO NOM FREQ.) 600a3

FIG. 6E

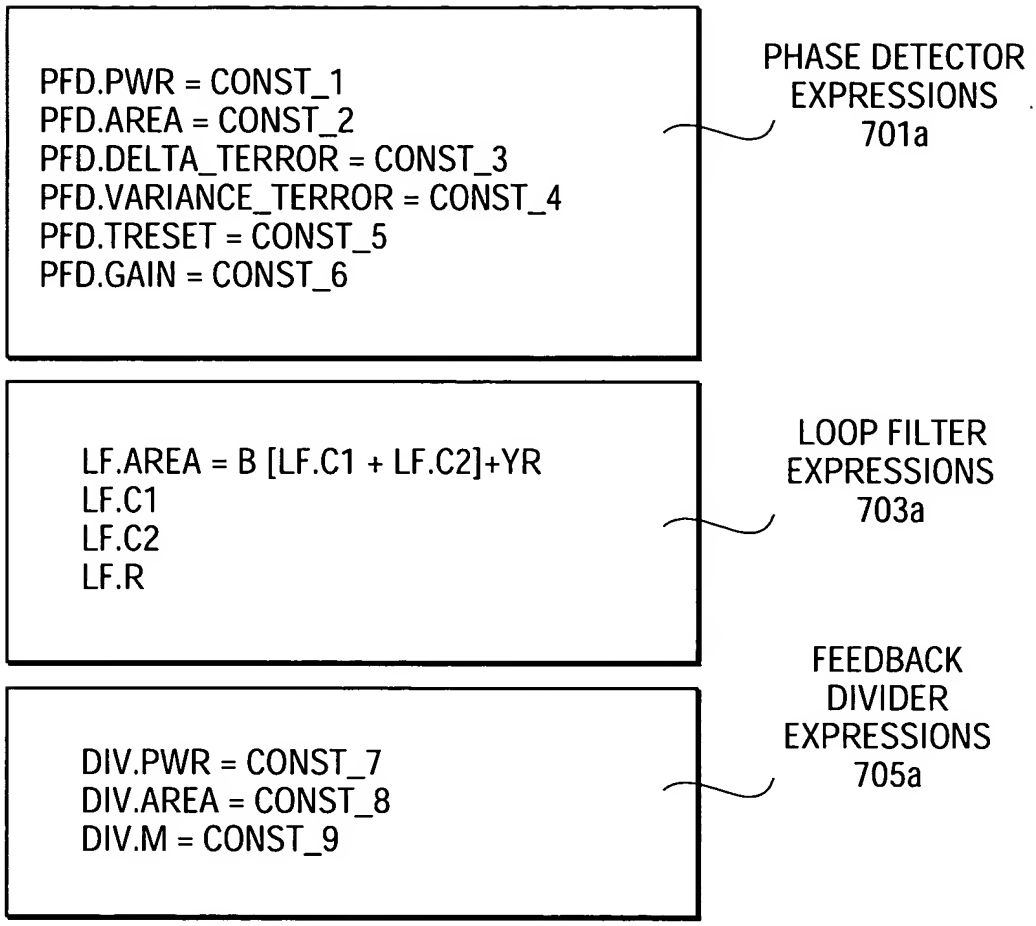

PFD.PWR = CONST_1
PFD.AREA = CONST_2
PFD.DELTA_TERROR = CONST_3
PFD.VARIANCE_TERROR = CONST_4
PFD.TRESET = CONST_5
PFD.GAIN = CONST_6
PHASE DETECTOR EXPRESSIONS 701a
LF.AREA = B [LF.C1 + LF.C2]+YR
LF.C1
LF.C2
LF.R
LOOP FILTER EXPRESSIONS 703a
DIV.PWR = CONST_7
DIV.AREA = CONST_8
DIV.M = CONST_9
FEEDBACK DIVIDER EXPRESSIONS 705a

FIG. 7A

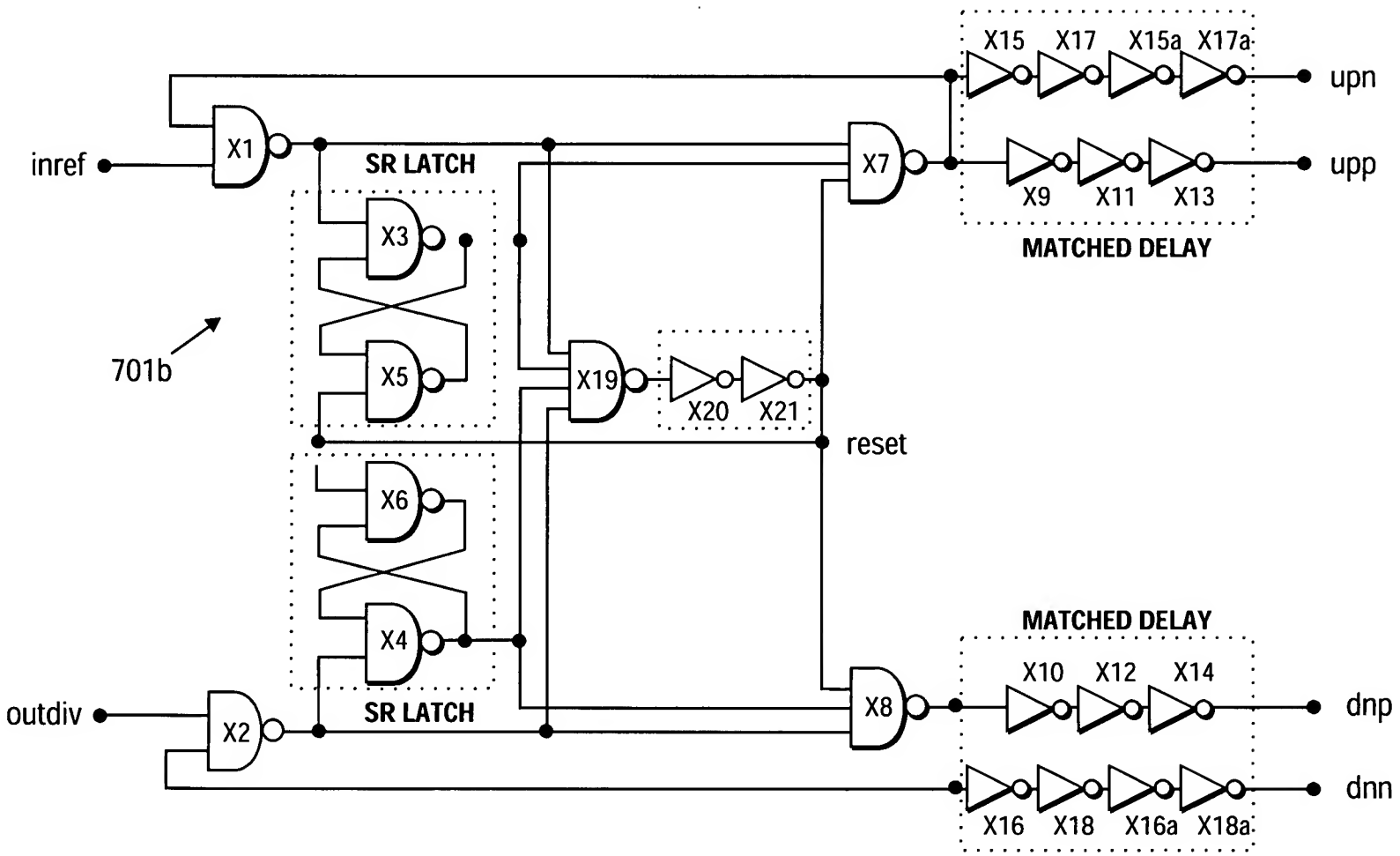

X15
X17
X15a
X17a
upn
upp
X9
X11
X13
MATCHED DELAY
inref
X1
SR LATCH
X7
X3
X5
701b
X19
X20
X21
reset
X6
X4
MATCHED DELAY
X10
X12
X14
outdiv
X2
SR LATCH
X8
dnp
dnn
X16
X18
X16a
X18a

FIG. 7B

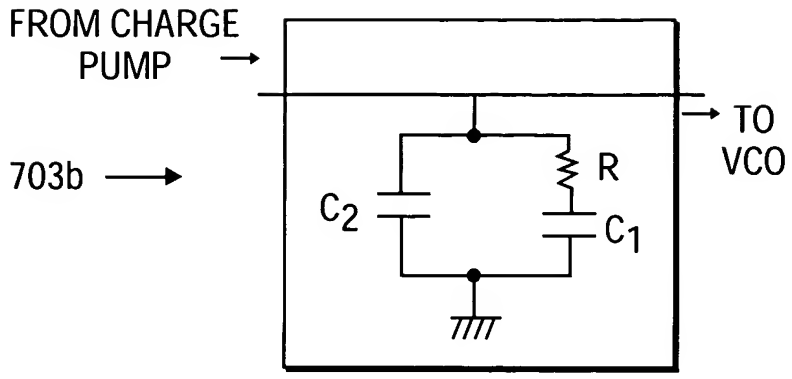



FIG. 7B (Cont.)

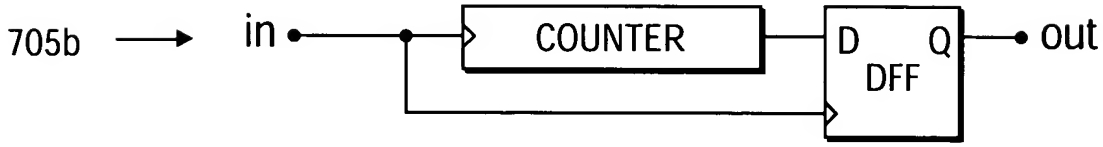



FIG. 7B (Cont.)

FIG. 8A

802A

$$CP.PWR = [4M9.ID + MS.ID]\, V_{DD} \longleftarrow 820$$

$$CP.IP = MS.ID \longleftarrow 821$$

$$CP.DELTA\_IP = \left[\frac{M5.gd\ (MG.gd)}{M6.gm} + \frac{M7.gd\ (M8.gd)}{M8.gm}\right]\frac{V_{DD}}{2} \longleftarrow 822$$

$$CP.IP\_VARIANCE = (MS.ID)^2\left(\frac{Z}{((M5.W)(M5.L)(M5.M))^{0.5}}\right)^2 + \left(\frac{DELTA.VT}{((M5.W)(M5.L)(M5.NF))^{0.5}}\right)^2 \bullet \left(\frac{1}{M5}\,\frac{}{gm}\right)^2$$
$$+ (M7.ID)^2\left(\frac{Z}{((M7.W)(M7.L)(M7.M))^{0.5}}\right)^2 + \left(\frac{DELTA.VT}{((M7.W)(M7.L)(M7.NF))^{0.5}}\right)^2 \bullet \left(\frac{1}{M7}\,\frac{}{gm}\right)^2 \Bigg\} 823$$

$$CP.DELTA\_QSTAT = \left[\frac{V_{DD}}{Z\ OPAMP.GAIN} + OMPAMP.DELTA\_VIN\right] \bullet \left[\left(\begin{array}{l} M6.Cdb + M6.Cgd + \\ 2M1.Cgs + 2M1.Cgd \end{array}\right) + \left(\begin{array}{l} MB.Cdb + Mi.Cgd + \\ 2M3.Cys + iM3.Cgd \end{array}\right)\right] \longleftarrow 824$$

$$CP.VARIANCE\_QSTAT = \left[\left(\begin{array}{l} M6.Cdb + M6.Cgd + \\ 2M1.Cgs + 2M1.Cgd \end{array}\right) + \left(\begin{array}{l} M8.Cdb + M8.Cgd + \\ 2M3.Cgs + 2M3.Cgd \end{array}\right)\right]^2 OPAMP.VARIANCE\_VIN \longleftarrow 825$$

$$CP.AREA = B\left[\begin{array}{l} W_5L_5 + W_{5a}L_{5a} + W_{5c}L_{5c} + W_6L_6 + W_{6a}L_{6a} + W_{6b}L_{b6} + W_{6c}L_{6c} + W_7L_7 + W_{7a}L_{7a} + W_{7b}L_{7b} + W_8L_8 \\ + W_{8a}L_{8a} + W_{8b}L_{8b} + W_{8c}L_{8c} + W_1L_1 + W_2L_2 + W_3L_3 + W_4L_4 + W_9L_9 + W_{10}L_{10} \end{array}\right] \Bigg\} 826$$
$$+ OPAMP.AREA + Iref.AREA$$

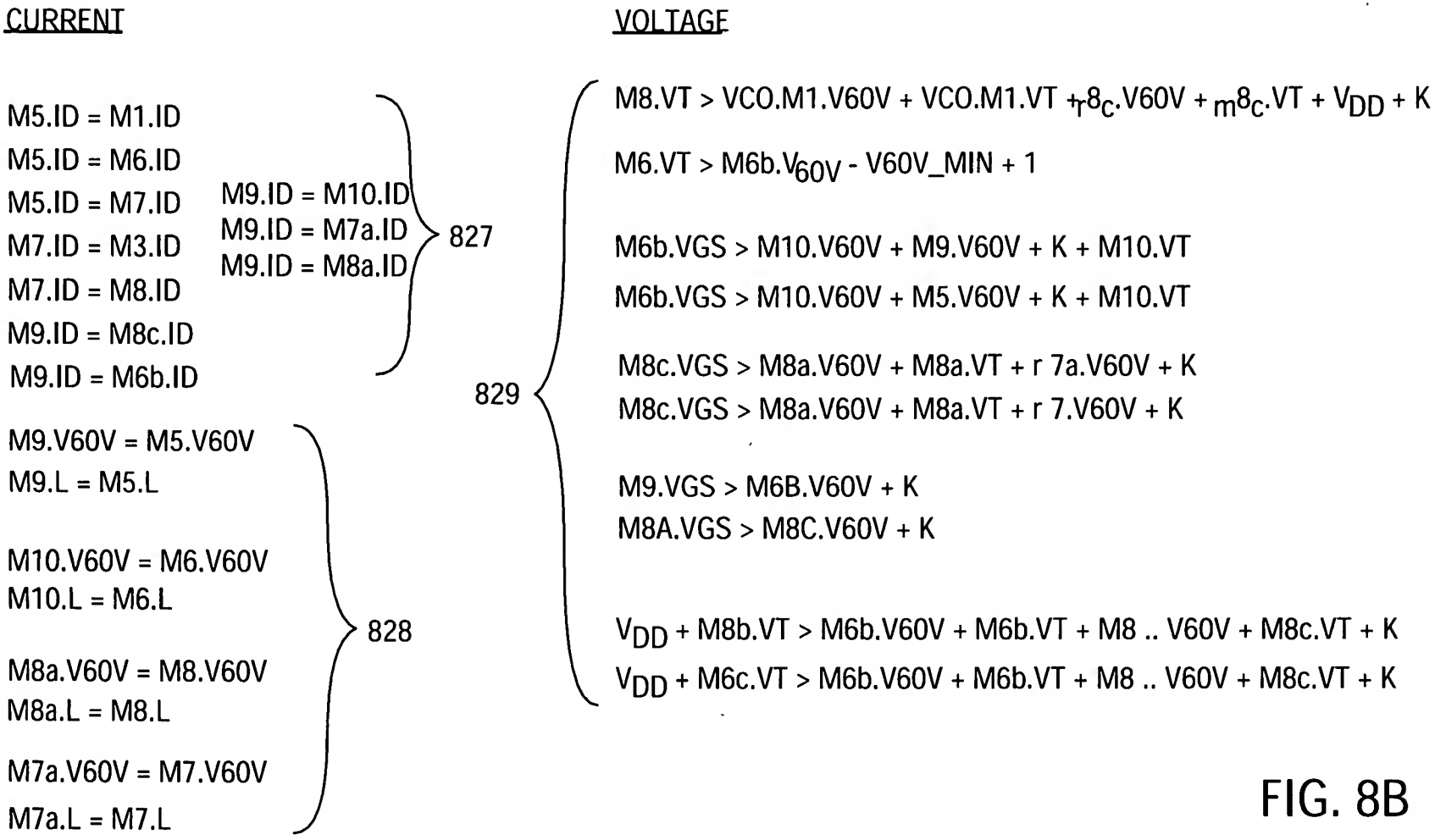

CURRENT
VOLTAGE
M5.ID = M1.ID
M5.ID = M6.ID
M5.ID = M7.ID
M7.ID = M3.ID
M7.ID = M8.ID
M9.ID = M8c.ID
M9.ID = M6b.ID
M9.ID = M10.ID
M9.ID = M7a.ID
M9.ID = M8a.ID
827
M9.V60V = M5.V60V
M9.L = M5.L
M10.V60V = M6.V60V
M10.L = M6.L
M8a.V60V = M8.V60V
M8a.L = M8.L
M7a.V60V = M7.V60V
M7a.L = M7.L
828
829
M8.VT > VCO.M1.V60V + VCO.M1.VT + T8C.V60V + m8C.VT + VDD + K
M6.VT > M6b.V60V - V60V_MIN + 1
M6b.VGS > M10.V60V + M9.V60V + K + M10.VT
M6b.VGS > M10.V60V + M5.V60V + K + M10.VT
M8c.VGS > M8a.V60V + M8a.VT + r 7a.V60V + K
M8c.VGS > M8a.V60V + M8a.VT + r 7.V60V + K
M9.VGS > M6B.V60V + K
M8A.VGS > M8C.V60V + K
VDD + M8b.VT > M6b.V60V + M6b.VT + M8 .. V60V + M8c.VT + K
VDD + M6c.VT > M6b.V60V + M6b.VT + M8 .. V60V + M8c.VT + K

FIG. 8B

802b

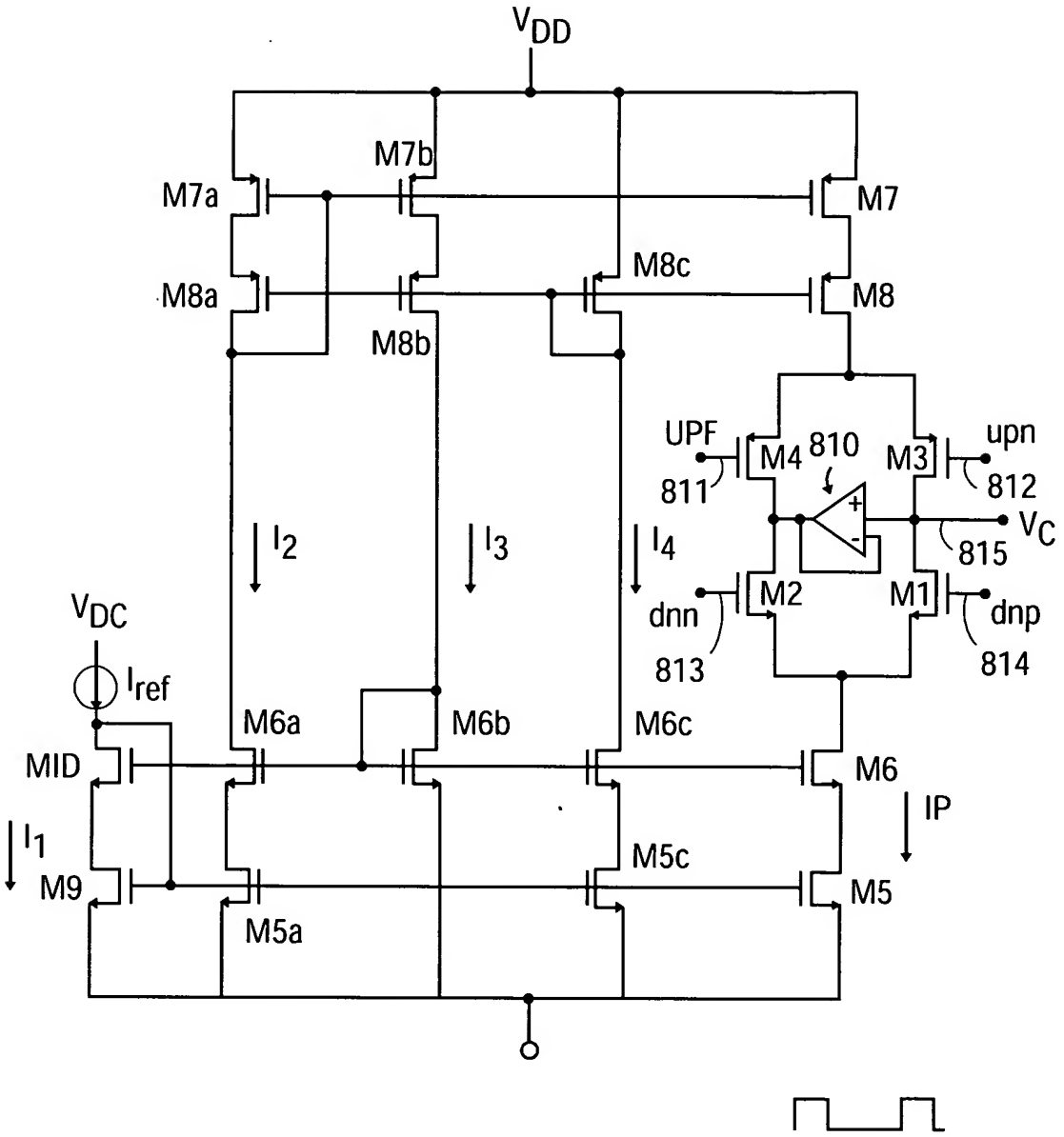

VDD
M7b
M7a
M7
M8c
M8a
M8
M8b
UPF
M4
810
M3
upn
811
812
VC
815
I2
I3
I4
VDC
dnn
M2
M1
dnp
813
814
Iref
M6a
M6b
M6c
MID
M6
IP
I1
M5c
M9
M5
M5a

FIG. 8C

$$VCO.PWR = (M21.ID + N(Mx.ID))V_{DD} + OPAMP.PWR \quad \leftarrow 920$$

$$VCO.AREA + OPAMP.AREA + W_{21}L_{21} + W_{22}L_{22} + W_{24}L_{24} + W_{25}L_{25} + \sum_{a=1}^{N} W_{ap}L_{ap} + \sum_{a\,1}^{r} W_{an}L_{an} + \sum_{a=1}^{N} W_{xa}L_{xa} \quad \leftarrow 921$$

$$VCO.GAW = 1/2\left[\frac{M21.gm\ (NMx.W)}{M22.W}\right]\left[\frac{(Mn+Mp)^{0.5}}{((Mn.ID)(Cnx(1+ratio))(Mn.W)N)^{0.5}(2Mn.L)^{1.5}}\right] \quad \leftarrow 922$$

$$VCO.KAPPA = \frac{\sqrt{z}(Mn.W)}{2 \cdot 6^{n.5}\ (n.75)\ N^{1.5}(Mp.W)(Mn.Cqs)(VCO.OUPUT\_FREQ)} \cdot \frac{4Nk^2T?\ [Mn.gm + Mp.gm]}{10[Mn.J]^{0.25}\ [Mn.L]^{0.25}\ [Mn.ID]^{0.25}} \quad \leftarrow 923$$

$$VCO.VDD\_DC = \frac{(Mn + Mp)^{0.5}}{((Mn.ID)(Cnx(1 + ratio))(Mn.W)N)^{0.5}\ (2L)^{1.5}} \cdot \frac{\left[\frac{1+N}{r_c} + N\ [M21\ gd + M22.gd]\right] \cdot \left[1 + \frac{M22.gd}{M22.gm}\right]}{OPAMP.GAIN} \quad \leftarrow 924$$

$$VCO.TAU3 = \frac{(M24.CGS)(M22.GM)}{(OPAMP.CM\_1>)(M22.GD)} \quad \leftarrow 925$$

FIG. 9A

CURRENT

926
- M21.ID = M22.ID
- M24.L = M22.L

927
- M22.V60V = Mx.V60V
- M22.L = Mx.L

928
- Mn.L = Mp.L
- Mp.W =(ratio) Mn.W

VOLTAGE

929 ⟶ $M22.V60V < V_{DD} - \frac{10(Mn.ID)^{0.25}(Mn.ID)^{0.25}}{(Mn.W)^{0.25}} - k$

930 ⟶ $M21.V60V < \frac{10(Mn.L)^{0.25}(Nn.ID)^{0.25}}{(Mn.W)^{0.25}} - k$

FIG. 9B

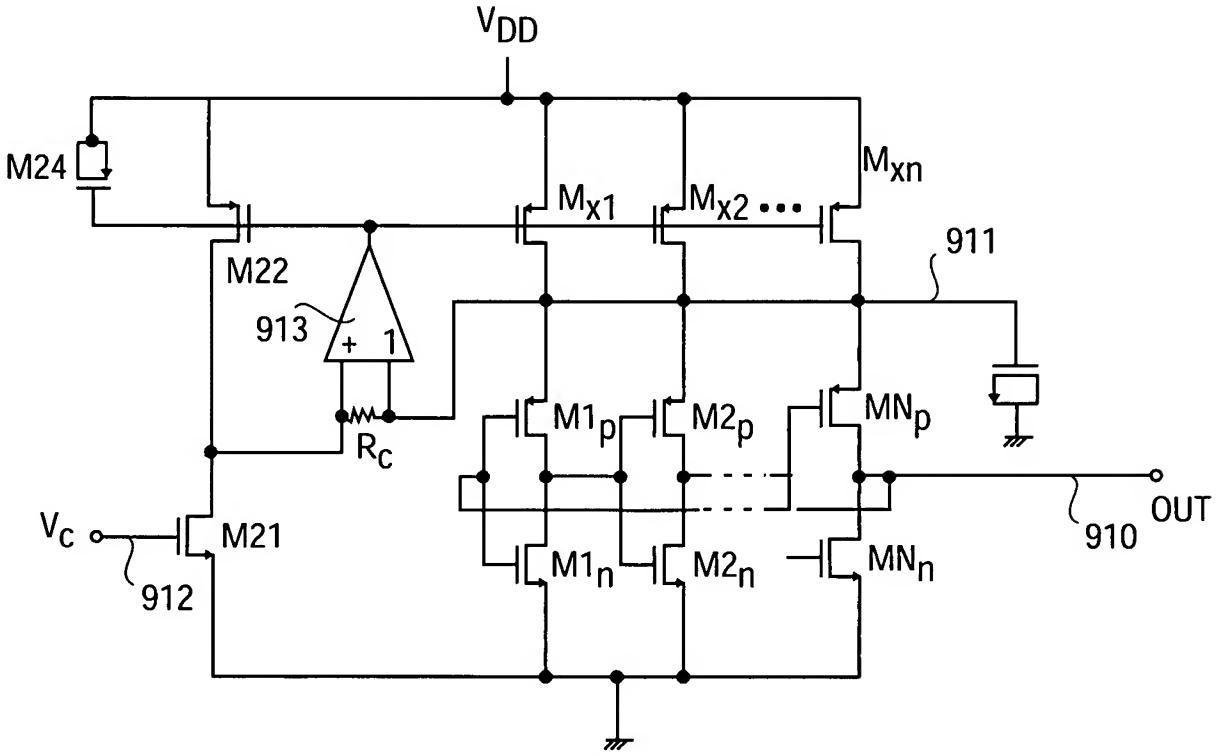

VDD
M24
M22
Mx1
Mx2 •••
Mxn
911
913
+ 1
Rc
M1p
M2p
MNp
Vc
M21
912
M1n
M2n
MNn
910
OUT

FIG. 9C

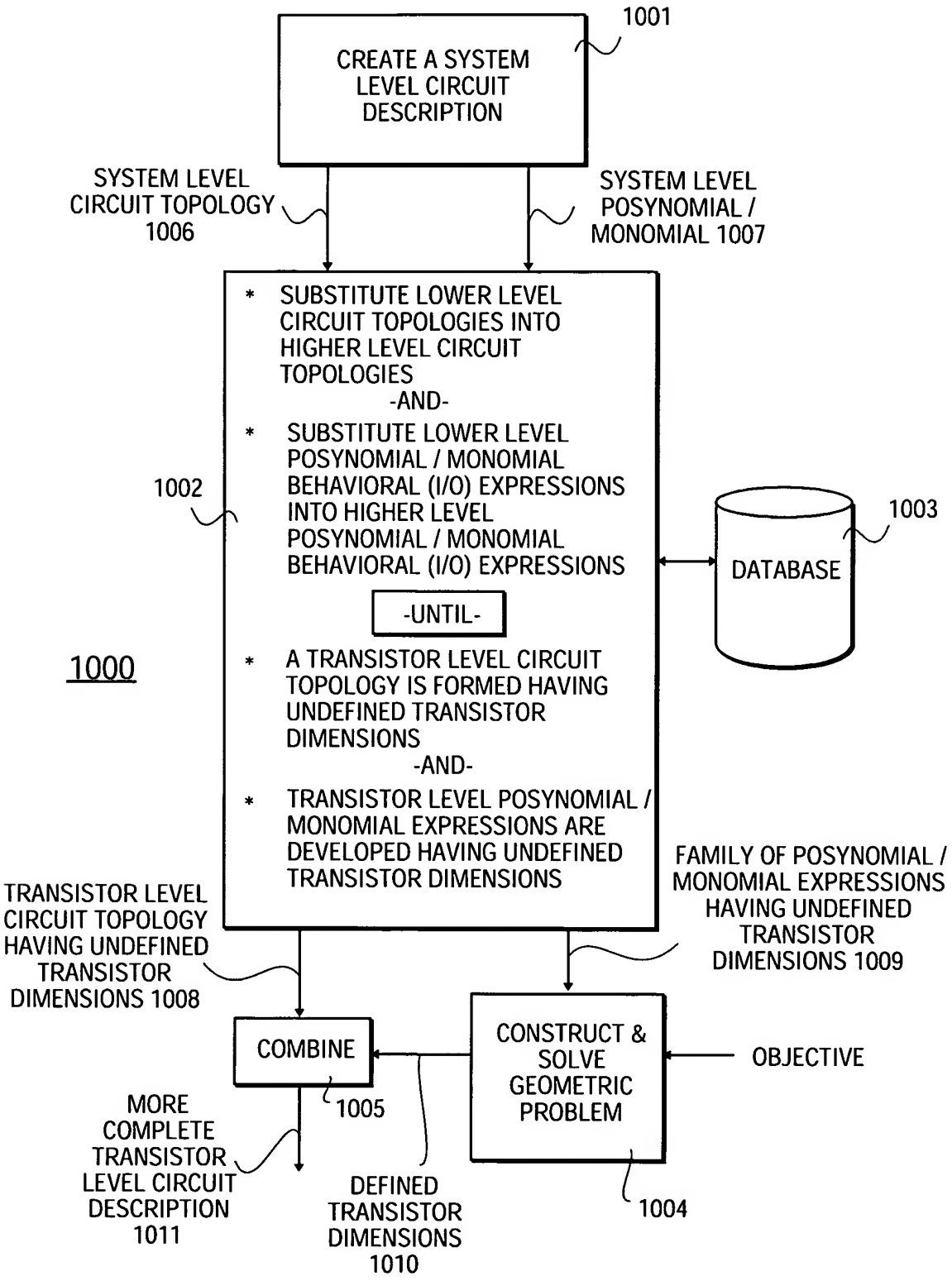

1001
CREATE A SYSTEM LEVEL CIRCUIT DESCRIPTION
SYSTEM LEVEL CIRCUIT TOPOLOGY 1006
SYSTEM LEVEL POSYNOMIAL / MONOMIAL 1007
* SUBSTITUTE LOWER LEVEL CIRCUIT TOPOLOGIES INTO HIGHER LEVEL CIRCUIT TOPOLOGIES
-AND-
* SUBSTITUTE LOWER LEVEL POSYNOMIAL / MONOMIAL BEHAVIORAL (I/O) EXPRESSIONS INTO HIGHER LEVEL POSYNOMIAL / MONOMIAL BEHAVIORAL (I/O) EXPRESSIONS
1002
-UNTIL-
* A TRANSISTOR LEVEL CIRCUIT TOPOLOGY IS FORMED HAVING UNDEFINED TRANSISTOR DIMENSIONS
-AND-
* TRANSISTOR LEVEL POSYNOMIAL / MONOMIAL EXPRESSIONS ARE DEVELOPED HAVING UNDEFINED TRANSISTOR DIMENSIONS
1000
DATABASE
1003
TRANSISTOR LEVEL CIRCUIT TOPOLOGY HAVING UNDEFINED TRANSISTOR DIMENSIONS 1008
FAMILY OF POSYNOMIAL / MONOMIAL EXPRESSIONS HAVING UNDEFINED TRANSISTOR DIMENSIONS 1009
COMBINE
1005
CONSTRUCT & SOLVE GEOMETRIC PROBLEM
1004
OBJECTIVE
MORE COMPLETE TRANSISTOR LEVEL CIRCUIT DESCRIPTION 1011
DEFINED TRANSISTOR DIMENSIONS 1010

FIG. 10

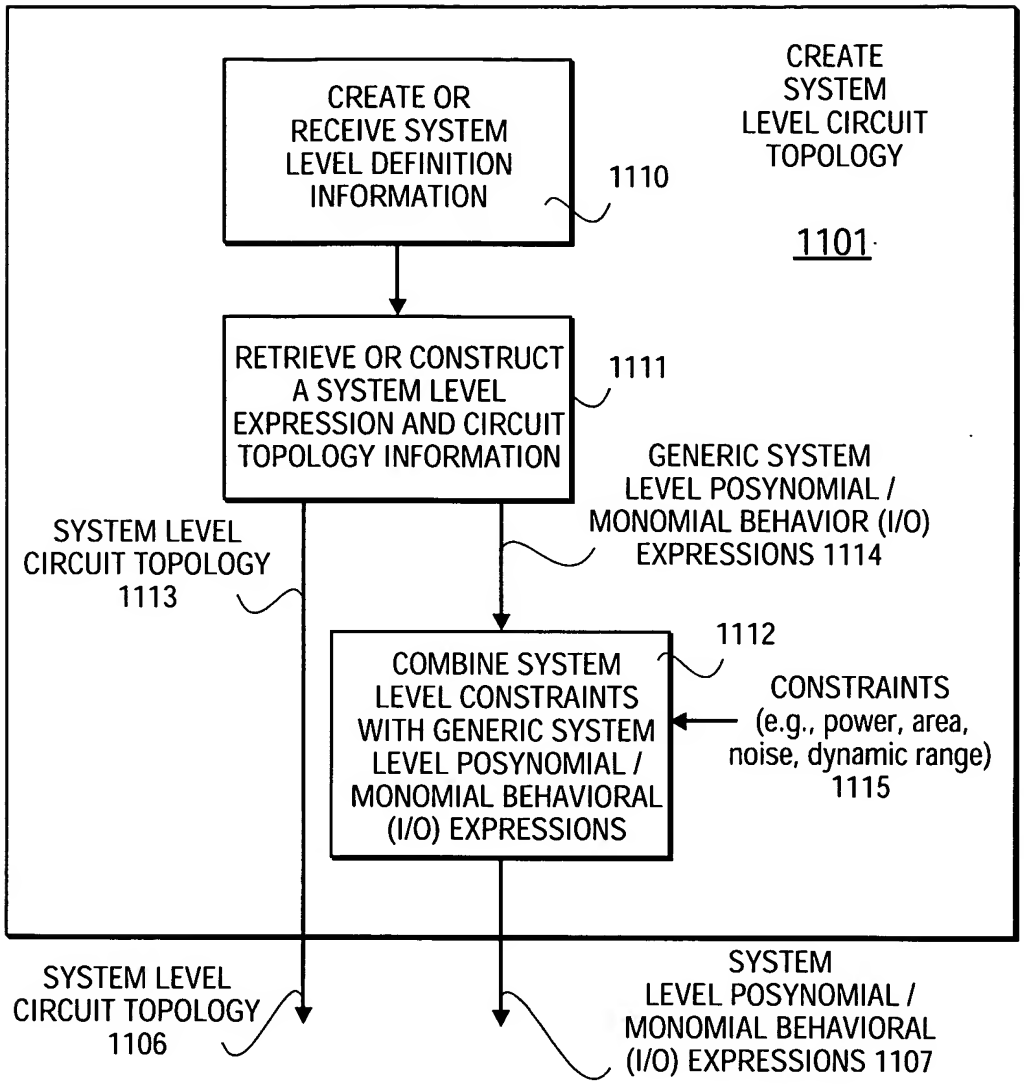

CREATE OR RECEIVE SYSTEM LEVEL DEFINITION INFORMATION
1110
CREATE SYSTEM LEVEL CIRCUIT TOPOLOGY
1101
RETRIEVE OR CONSTRUCT A SYSTEM LEVEL EXPRESSION AND CIRCUIT TOPOLOGY INFORMATION
1111
GENERIC SYSTEM LEVEL POSYNOMIAL / MONOMIAL BEHAVIOR (I/O) EXPRESSIONS 1114
SYSTEM LEVEL CIRCUIT TOPOLOGY 1113
1112
COMBINE SYSTEM LEVEL CONSTRAINTS WITH GENERIC SYSTEM LEVEL POSYNOMIAL / MONOMIAL BEHAVIORAL (I/O) EXPRESSIONS
CONSTRAINTS (e.g., power, area, noise, dynamic range) 1115
SYSTEM LEVEL CIRCUIT TOPOLOGY 1106
SYSTEM LEVEL POSYNOMIAL / MONOMIAL BEHAVIORAL (I/O) EXPRESSIONS 1107

FIG. 11

SYSTEM LEVEL: PLL.PWR = PFD.PWR + CP .PWR + VCO.PWR + DIV.PWR

AFTER SUBSTITUTION OF LOWER LEVEL
INFORMATION FOR
CP.PWR & VCO.POWER:

1210 → PLL.PWR = PFD.PWR + [4M9.ID + M5.ID] $V_{DD}$ + M21.ID + N(Mx.ID) $V_{DD}$ + OPAMP.PWR

FIG. 12

PFD

CP

VCO

DIV

R

C1

C2

1 = PFD.VDD; CP.VDD; VCO.VDD; DIV.VDD

2 = PFD.GND; CP.GND; C1.2; C2.2; VCO.GND; DIV.GND

3 = PFD.IN_1

4 = PFD.OUT_UP; CP.IN_UP

5 = PFD.OUT_DOWN; CP.IN_DOWN

6 = CP.OUT; C2.1; R.1; VCO.IN

7 = R.2; C1.1

8 = VCO.OUT; DIV.IN

9 = DIV.OUT; PFD.IN_2

FIG. 13

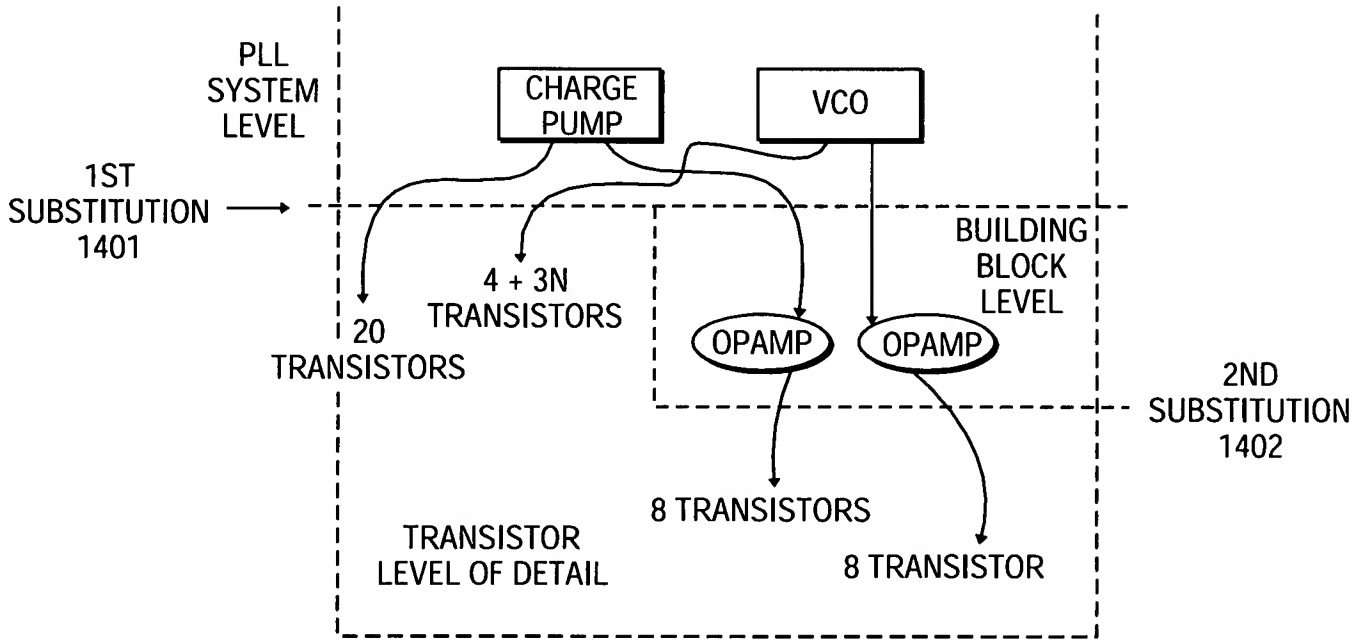

PLL
SYSTEM
LEVEL
CHARGE
PUMP
VCO
1ST
SUBSTITUTION
1401
BUILDING
BLOCK
LEVEL
4 + 3N
TRANSISTORS
20
TRANSISTORS
OPAMP
OPAMP
2ND
SUBSTITUTION
1402
8 TRANSISTORS
TRANSISTOR
LEVEL OF DETAIL
8 TRANSISTOR

FIG. 14

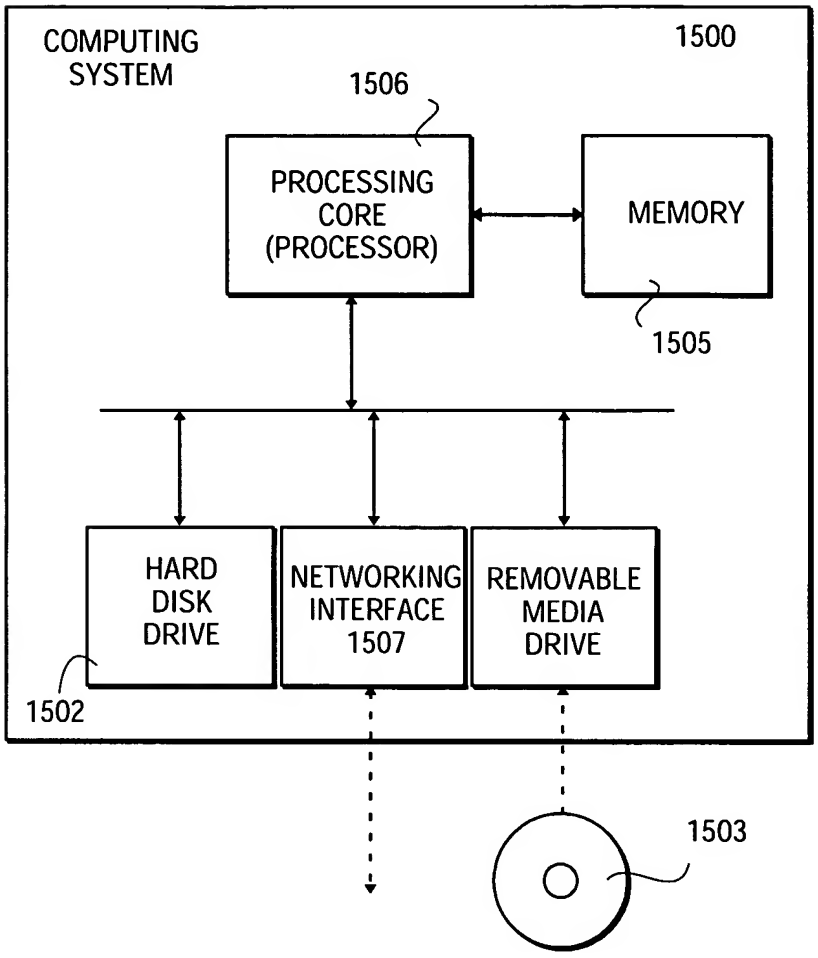

COMPUTING SYSTEM
1500
1506
PROCESSING CORE (PROCESSOR)
MEMORY
1505
HARD DISK DRIVE
NETWORKING INTERFACE 1507
REMOVABLE MEDIA DRIVE
1502
1503

FIG. 15